WHAT IS CLAIMED IS:

1. In an integrated circuit multiprocessor switching device, an apparatus for mapping a plurality of interrupt sources from a plurality of data channels to a plurality of processors, comprising:

a first interrupt status register for storing at least one interrupt source for a first data channel;

a second interrupt status register for storing at least one interrupt source for a second data channel;

an interrupt indication register associated with each data channel for storing a merged interrupt value representing said at least one interrupt source for the associated data channel, where each interrupt indication register is combined to form a merged interrupt status register;

an interrupt mapping register associated with each data channel for storing a processor identification for each associated data channel;

for each data channel, a demultiplexing circuit coupled to the merged interrupt status register and the interrupt mapping register associated with the data channel for coupling the merged interrupt value for the each data channel to a processor identified by the processor identification.

2. The apparatus recited in claim 1 formed in a packet manager input circuit for mapping a plurality of interrupt sources from a plurality of input channels such that the first data channel comprises a first input channel and the second data channel comprises a second input channel.

3. The apparatus recited in claim 1 formed in a packet manager output circuit wherein the first data channel comprises a first output virtual channel and the second data channel comprises a second output virtual channel.

4. The apparatus recited in claim 1 formed in a system controller wherein the plurality of data channels comprises at least one input channel having a first plurality of interrupt sources and at least one output channel having a second plurality of interrupt

sources and wherein the merged interrupt status register comprises a first interrupt indication register associated with said at least one input channel for storing a merged interrupt value representing the first plurality of interrupt sources and a second interrupt indication register associated with said at least one output channel for storing a merged interrupt value representing the second plurality of interrupt sources.

5. The apparatus recited in claim 1, further comprising a first mask register for selectively masking the at least one interrupt source for the first data channel, wherein the merged interrupt value comprises a masked merged interrupt value.

6. The apparatus recited in claim 5 wherein the first mask register is programmable to select which interrupt source is masked.

7. The apparatus recited in claim 1, wherein the processor identified by the processor identification determines an interrupting channel by running an interrupt service routine that first reads the merged interrupt status register to identify which data channel generated the interrupt and then reads the interrupt status register corresponding to the identified data channel to determine the interrupt source for the interrupting channel.

8. The apparatus recited in claim 1, wherein each interrupt mapping register further comprises a priority level indication associated with each data channel for prioritizing any interrupt issued by the data channel, whereby the demultiplexing circuit selectively couples the merged interrupt value for the each data channel to a plurality of prioritized processor interrupt signals under control of the processor identification and priority level indication.

9. An interrupt mapper for mapping interrupts from a plurality of channels to a plurality of processing cores, comprising:

a plurality of source registers, where each source register identifies interrupt sources for one of the plurality of channels;

a mask register associated with each of the plurality of source registers for selectively masking said associated source register to generate masked interrupt sources for each channel;

a channel merge circuit for merging the masked interrupt sources for each channel into an interrupt indication value for said channel;

a channel register that stores the interrupt indication values for the plurality of channels;

a plurality of processor map storage devices, each processor map storage device storing a processor identification value for one of the plurality of channels; and

a demultiplexer coupled to the channel register and the plurality of processor map storage devices for mapping each interrupt indication value for a channel to a processing core identified by the processor identification for that channel.

10. The interrupt mapper as recited in claim 9, further comprising a plurality of AND gates coupled to the source registers and mask registers for generating the masked interrupt sources for each channel.

11. The interrupt mapper as recited in claim 9, wherein each processor map storage device stores a processor identification value and a priority level for one of the plurality of channels.

12. The interrupt mapper as recited in claim 9, wherein the channel merge circuit comprises OR gate circuitry for merging the masked interrupt sources into an interrupt indication value for each channel.

13. The interrupt mapper as recited in claim 9, wherein a processing core that receives an interrupt reads the channel register to determine which channel generated the interrupt and then reads the plurality of source registers to determine a source for the channel's interrupt.

14. The interrupt mapper as recited in claim 13, wherein the plurality of source registers and the channel register are each sized to match a processing width of the processing core.

15. The interrupt mapper as recited in claim 14, wherein the processing core determines the source of an interrupt with two register reads.

16. The interrupt mapper as recited in claim 9, wherein interrupts from each channel are mapped to only one processing core.

17. The interrupt mapper as recited in claim 9, wherein the plurality of processor map storage devices are programmable to dynamically assign channel interrupts to the processing cores to implement load balancing among the processing cores.

18. A method for processing interrupts from a plurality of channels to a plurality of processing cores in an integrated circuit multiprocessor, comprising:

receiving a mapped interrupt signal at a first processor core;

reading a merged interrupt status register to identify an issuing channel from the plurality of channels that issued the mapped interrupt signal;

reading an interrupt source register for the issuing channel to determine an interrupt source; and

processing the interrupt source specified in the interrupt source register for the issuing channel.

19. The method of claim 18, further comprising reading a single status register containing interrupt sources for a plurality of active channels to identify the interrupt source when all possible interrupt sources from the plurality of active channels can be stored in the single status register.

20. The method of claim 18, further comprising:

masking a plurality of interrupt sources for each channel;

for each channel, merging the masked plurality of interrupt sources to an interrupt indication value;

storing the interrupt indication value for each channel in the merged interrupt status register;

mapping the interrupt indication value for each channel to the mapped interrupt signal under control of a processor identification value assigned to each channel.